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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,007	12/04/2001	William R. Wheeler	10559-606001/P12890	9720

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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,007	WHEELER ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/12/2003, 3/22/2002, 6/11/2003, 3/15/2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 29 have been examined. Claims 1 – 29 have been rejected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 6 and 13 - 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

3.1. Regarding claims 1 and 13:

3.1.1. Watkins appears to teach a method and machine-accessible medium using a logic design element in a logic design (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

3.1.2. Watkins appears to teach a method and machine-accessible medium performing a simulation of the logic design that includes simulating the logic design element (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

3.1.3. Watkins appears to teach a method and machine-accessible medium having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 - 49***).

3.2. Regarding claims 2 and 14:

3.2.1. Watkins appears to teach displaying the instrumentation data relating to the logic design element (***Figure 3***).

3.3. Regarding claims 3 and 15:

3.3.1. Watkins appears to teach receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

3.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

3.4. Regarding claims 4 and 16:

3.4.1. Watkins appears to teach displaying the instrumentation data after performing the simulation (***column 5, lines 14 – 16***).

3.5. Regarding claims 5 and 17:

3.5.1. Watkins appears to teach displaying the instrumentation data while performing the simulation (***column 7, lines 48 – 57***).

3.6. Regarding claims 6 and 18:

3.6.1. Watkins appears to teach performing the simulation means performing a partial simulation (***column 7, lines 12 – 27***).

3.6.2. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the partial simulation (***column 7, lines 24 – 27***).

3.6.3. Watkins appears to teach displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation (***column 7, lines 12 – 27***).

4. Claims 25 -27 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

4.1. Regarding claim 25:

4.1.1. Watkins appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

4.1.1.1. Regarding (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***); figure 2, element 224, is a simulation module.

4.1.2. Watkins appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect instrumentation data relating to the logic design element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column***

10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27).

4.1.2.1. Regarding (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***); Watkins teaches software that collects data, therefore it would have been inherent that the software has a portion of code to collect data, which is a collection module.

4.2. Regarding claim 26:

4.2.1. Watkins appears to teach a display module that is structured and arranged to display the instrumentation data relating to the logic element design (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***).

4.2.1.1. Regarding (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***); Column 7, lines 12 – 19, recites that the simulation module displays the instrumentation data; therefore the logic simulator (***figure 2, element 224***) is a display module.

4.3. Regarding claim 27:

4.3.1. Watkins appears to teach an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the design element, wherein the display module is structured and arranged to display the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

4.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query. Watkins teaches software to receive a query, therefore it is

inherent that there is a portion of code that receives the query, which is an interface module to receive the query.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 – 9 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Sharma (U.S. Patent 5,978,574).

6.1. Claim 7 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

6.2. Claim 19 is a dependent claim of claim 13, and thereby inherits all of the rejected limitations of claim 13.

6.3. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

6.4. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

6.5. Regarding claims 7 and 19:

6.5.1. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating

to the logic element (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

6.5.2. Watkins does not specifically teach that ***the logic design element includes a FIFO memory***, and having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***FIFO memory***.

6.5.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

6.5.4. The motivation to use the art of Sharma with the art of Watkins is the statement recited in Sharma that verification of queue flow control is traditionally performed through simulation (***column 2, lines 10 – 14; and column 2, lines 31 – 36***).

6.6. Regarding claims 8 and 20:

6.6.1. Watkins appears to teach having the logic elements record usage during the simulation (***figure 4; and column 5, lines 5 – 10; and column 6, lines 45 – 52; and column 7, lines 32 – 35***).

6.6.2. Watkins does not specifically teach having the ***FIFO memory*** record usage ***of the FIFO memory*** during the simulation.

6.6.3. Sharma appears to teach a FIFO memory simulation (***figure 2; and column 2, lines 10 – 13; and column 1, lines 31 – 35***).

6.7. Regarding claims 9 and 21:

6.7.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

6.7.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

6.7.2. Watkins appears to teach displaying the instrumentation data relating to the logic element in response to the query (***column 7, lines 36 – 45***).

6.7.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***FIFO memory***.

6.7.4. Watkins does not specifically teach displaying the instrumentation data relating to ***the FIFO memory*** in response to the query.

6.7.5. Sharma appears to teach a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

6.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Sharma with the art of Watkins to produce the claimed invention.

7. Claims 10 - 12 and 22 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Mitchell (U.S. Patent 5,646,553).

7.1. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

7.2. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

7.3. Regarding claims 10 and 22:

7.3.1. Watkins appears to teach that having the logic element automatically collect the instrumentation data includes having the logic element automatically collect the

instrumentation data during the simulation, with the instrumentation data relating to the logic element (***column 7, lines 12 – 17***).

7.3.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

7.3.3. Watkins does not specifically teach having the logic element automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***tri-state bus***.

7.3.4. Mitchell appears to teach that a logic design includes a tri-state bus (***Abstract, and figure 1***).

7.3.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 – 50***).

7.4. Regarding claims 11 and 23:

7.4.1. Watkins appears to teach that having a logic element automatically collect the instrumentation data includes having a logic element automatically collect usage of a logic element during the simulation (***column 7, lines 11 – 26; column 6, lines 45 – 53***).

7.4.2. Watkins does not specifically teach that having the ***tri-state bus*** automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect usage of the ***tri-state bus*** during the simulation.

7.4.3. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

7.5. Regarding claims 12 and 24:

7.5.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

7.5.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

7.5.2. Watkins appears to teach displaying the instrumentation data relating to a logic element in response to the query (***column 7, lines 36 – 45***).

7.5.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***tri-state bus***.

7.5.4. Watkins does not specifically teach displaying the instrumentation data relating to the ***tri-state bus*** in response to the query.

7.5.5. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

8. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Sharma (U.S. Patent 5,978,574).

8.1. Claim 28 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

8.2. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

8.3. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

8.4. Regarding claim 28:

8.4.1. Watkins appears to teach that the collection module is integrated with the logic design element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

8.4.2. Watkins does not specifically teach that the collection module is integrated with the ***FIFO memory*** and is structured and arranged to automatically collect the instrumentation data relating to the ***FIFO memory*** during the simulation.

8.4.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

8.4.4. The motivation to use the art of Sharma with the art of Watkins is the statement recited in Sharma that verification of queue flow control is traditionally performed through simulation (***column 2, lines 10 – 14; and column 2, lines 31 – 36***).

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Mitchell (U.S. Patent 5,646,553).

9.1. Claim 29 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

9.2. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

9.3. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

9.4. Regarding claim 29:

9.4.1. Watkins appears to teach that the collection module is integrated with the logic element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***column 7, lines 12 – 17***).

9.4.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

9.4.3. Watkins does not specifically teach that the collection module is integrated with the ***tri-state bus*** and is structured and arranged to automatically collect the instrumentation data relating to the ***tri-state bus*** during the simulation.

9.4.4. Mitchell appears to teach that a logic design element includes a tri-state bus (***Abstract, and figure 1***).

9.4.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 – 50***).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-262-3749. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. Thomson
Primary Examiner
TC 2100
Aug 2005

RG